Resume: Tom Morrison

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Professional Summary

- More than 25 years of experience in Consumer, Network/Telecom, PC core, 3D graphics, DoD and Simulation & Training industries
- Expert in Application Specific Integrated Circuit (ASIC), Field Programmable Gate Array (FPGA) and System design, verification, synthesis and test including Xilinx, Altera, digital, analog, mixed-signal, Radiation Tolerant for Space, DFT, JTAG, ATM, DSP, embedded processors (ARM w/ AMBA Lite, PowerPC), DDR DRAM, IEEE1394 (Firewire), Pentium, Homeplug, PCI, AGP, IDE, ATAPI, LPC, PLL, DAC, ADC and digital video standards (CCIR/SMPTE) for 5,000,000+ gate designs
- Specific deep expertise in verification via simulation and FPGA-based emulation with System Verilog, Vera, OVM and UVM
- Project Engineering, Proposal and Cost Estimating, Design Process improvement and automation, Design tool training, 3D modeling
- *Proficiencies*: Verilog, VHDL, Xilinx ISE/EDK, Altera Quartus, Vera, System Verilog, XL, VCS, ModelSim, Open Verification Methodology (OVM), Synopsys Synthesis and Primetime, Layout and Routing, Timing Analysis and Closure, Floorplanning, ClearCase, Perforce, SCCS, RCS, Java, Matlab, C/C++, Perl, Tcl, Assembly, Unix, Windows, Cadence, Quartus, Synplicity, and MS Office

Experience

- **November 2010 to present Intelliform Internal Projects** – Accomplished various business development efforts including IP development and additional formal verification training in System Verilog and OVM.
- **March 2006 to November 2010 Consultant to Northrop Grumman** – Provided design expertise for development of an Airborne Standoff Mine Detection Sensor (ASTAMIDS). The sensor also included Reconnaissance, Search, and Target Acquisition (RSTA) capabilities. Designed with significant size/weight restrictions, the sensor is specifically intended for use on the FireScout unmanned helicopter developed for the Army and Navy. My responsibilities were for the sensor controller system design and Xilinx FPGA that included multiple PowerPC's, JPEG 2000 compression, flash disk storage, multiple Gigabit Ethernet interfaces, DDR DRAM (2), and Matlab-to-'C' conversion for embedded software.
- **November 2009 to July 2010 Consultant to Northrop Grumman** – Developed Xilinx FPGA circuits for upgrades to the Airborne Laser Mine Detection System (ALMDS). The sensor uses an active scanning laser to identify potential marine mines. System is currently fielded by the U.S. Navy. Converted 'C' and Matlab image analysis algorithms to real-time hardware circuits in a Xilinx Virtex 4 FPGA.
- **February 2010 to June 2010 Consultant to Aeronix** – Accomplished system-level design for DARPA F6 Fractional Satellite. Defined architecture to implement several functions in a radiation-tolerant Xilinx Virtex 5 FPGA. FPGA provided all support functions for Leon3FT processor.
- **July 2009 to August 2009 Consultant to Intellon (now Qualcomm)** – Verified ASIC implementation of Ethernet MAC/PHY interface (GMII/RGMII) with Xilinx FPGA.
- **July 2007 to January 2008 Consultant to Intellon (now Qualcomm)** – Developed Xilinx FPGA design for NallaTech FPGA emulation product. This design supports an R&D effort to explore means

to increase data transfer rates for Homeplug AV compliant Powerline Network. Implemented Matlab functions in FPGA to improve research capabilities.

- **May 2003 to March 2006 Consultant to Intellon (now Qualcomm)** – Led verification and testing of a Homeplug AV compliant Powerline Network PHY. Developed VHDL verification environment and designed interfaces for Xilinx FPGA-based prototype. Created verification strategy and environment in Tcl that integrated Verilog/Matlab simulation and FPGA emulation of the production PHY design. Utilized System Verilog with Open Verification Mehodology (OVM) to define assertions and construct verification environment. Led the development of key interfaces for the production PHY. ASIC was implemented in .9μ TSMC process and utilized ARM 7 processor with AMBA Lite bus protocol. ASIC contained about 12 million gates including 3072 point and 396 point FFT/IFFT's, Turbo Code Forward Error Correction, and 128-bit AES encryption.

- **November 2001 to August 2002 Development Contract for Sega** - Designed and implemented an FPGA and Intellectual Property (IP) for an ASIC to integrate Microsoft's XBox with Sega's Arcade data storage subsystem. Accomplished all design aspects from system design through prototype test. Design utilized IDE/ATAPI (ATA 100) and LPC bus interfaces. Accomplished design and verification in Verilog. Implemented the design on Altera FPGA with Quartus and Synplicity software. Accomplished test with XBox Development kit and Intelliform's test equipment (HP Logic Analyzer and Tektronix Digital Storage Oscilloscope).

- **July 2001 to January 2002 Consultant to Sony** - Designed and implemented a Digital Signal Processor to accomplish Watermark insertion for a Digital Copyrights Protection ASIC. Digital video input/output was in CCIR656 parallel digital video format. Developed the system design based on a reference design in VHDL. Accomplished the design and verification in Verilog. Implemented a prototype of the entire ASIC (300,000 gates plus 29 K-bits of internal SRAM) in a set of Altera Apex FPGA's with Synplicity. Established digital video test lab for the new design group (VTR's, Logic Analyzers, DSO's, Serial/Parallel digital video conversion (SMPTE standards). Formed and executed the prototype test plan. ASIC was implemented in .13μ TSMC process.

- **May 2000 to June 2001 Consultant to Nortel** - Designed and implemented a data storage and retrieval circuit for a queuing manager ASIC in a high-speed router switch. The circuit handled ATM cell data and IP frame data. It utilized embedded DRAM for linked list storage and stored the data in external SDRAM. Performed top-level architecture tradeoffs in C/C++. Accomplished the design and block level verification in Verilog. Assisted emulation team to emulate the entire ASIC in Xilinx FPGA's. ASIC contained 500,000 gates plus 312 M-bits of embedded DRAM and 72 K-bits of SRAM.

- **November 1998 to May 2000 Consultant to Nortel** - Verified multiple, programmable Digital Signal Processors for a large ASIC in a Terabit router switch. Assisted with system design and RTL (Verilog) coding. Developed a verification plan to ensure correct operation on ATM and Frame Relay packets. Verified the processors with Vera. Wrote Perl program to generate firmware for verification. Synthesized the design for .18μ TI process with Synopsys. Accomplished formal verification with Chrysalis and timing verification with Synopsys Primetime.

- **May 1998 to September 1998 Consultant to Synopsys** – Served as a Synopsys consultant to a Synopsys customer to implement synthesis for a Gigabit Ethernet ASIC. Mentored the design team on how to code for synthesis. Developed the synthesis scripts from scratch.

- **March 1997 to March 1998 Consultant to National Semiconductor** – Verified an IEEE 1394 PHY ASIC. Mentored the design team in Verilog coding techniques. Verified a Pentium North-bridge support ASIC. SoC ASIC included CPU, main memory (SDRAM), PCI, and AGP interfaces on an internal system bus. Developed the verification plans and accomplished the verifications with Verilog.

- **November 1996 to February 1997 Consultant to Sega** – Performed early architecture analysis and tradeoffs for Saturn home video product.

- **July 1996 to October 1996 Development Contract for Sega** – Developed Verilog IP modules to accomplish 3-D Graphics math functions such as 1/x, sin(x), invtan(x).

- **1989 to 1996 GE, Lockheed Martin, Real 3D** – Led engineering teams of 5 to 25 people in the development of real-time, 3-D, Computer graphics systems for use in the entertainment industry. Accomplished Circuit Card design and test. Accomplished RTL coding and verification in primarily in Verilog with some modules in VHDL. Company sold more than two times the number of systems that marketing projections predicted. Introduced RTL simulation into standard product development process. Received two Managerial awards for these projects.
- **1988 GE** – Established a proposal cost estimating process which simplified the task and provided consistently repeatable estimates. Subsequent measurements found the process to provide estimates that were usually within 10% of the actual costs incurred.
- **1984 to 1988 GE** – Co-directed a 25 person team on the development of a Computer graphics system for the Aerospace Simulation & Training industry. Accomplished Circuit Card design and test. Developed 3-D graphics firmware for DSP's. Produced 3D modeling databases for flight simulation and related applications. Received Managerial award for process improvements.
- **1983 to 1984 GE** – Initiated and promoted the use of workstations and design tools for ASIC and system design. Achieved a 90% first pass success rate with ASIC's. Reduced product design cycles by average of 20% per year.

Employment History

1996 - Present: *President & Consultant*, **Intelliform Corp**.

1983 - 1996: *Design Engineer to Senior Staff Engineer*, **GE – Real 3D (Lockheed Martin)**

Education

GE Managerial Preparation Courses

MS Computer Engineering, 1989 from *National Technological University*

BS Electrical Engineering, 1983 from the *University of Florida*; Graduated with Honors

Publications

1987: *The Unified Automated Design Environment* - GE Aerospace CADMAT News - February

1986: Benefits of Design Automation - Design Systems for Electrical and Electronics Engineering Conference, San Francisco, CA